11 GHz BANDWIDTH GaAs MESFET/MSM OEIC RECEIVERS

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Abstract

We report state-of-the-art performance of direct ion implanted GaAs-MESFET with a 0.6 μm gate length and MSM based OEIC receiver achieving a -3 dB bandwidth as high as 11 GHz for optical signals at the wavelength of 850 nm. The feedback resistance of the receiver is 1000 Ω and the effective transimpedance is 565 Ω into a 50 Ω load. The effective transimpedance-bandwidth (TZBW) product is 6.1 THz-Ω for this receiver.

1. INTRODUCTION

OEIC receivers for optical signals with the wavelength of 850 nm or less have been developed over the past 10 years [1-3]. The best reported OEIC receiver bandwidth of GaAs MESFET-MSM is 5.2 GHz [2] and of GaAs/AlGaAs HEMT-MSM is 8.2 GHz [3]. Optical interconnects are vital to ultra-high speed digital communication and computing systems. However, the insertion of optical interconnects into a system can only be realized if optoelectronic integrated circuit (OEIC) chips for generating, transmitting, processing, and receiving optical signals can be made cost effective. To achieve the goals of affordability and availability, our work has focused in developing a robust ion-implanted GaAs MESFET based IC process for fabricating low cost OEIC chips. Direct ion implantation of LEC substrates for GaAs MESFET was first reported in 1982 [4], and subsequently ultra-high performance GaAs MESFET achieving a unity current gain cutoff frequency above 100 GHz, were reported in 1992 [5]. In this work, we wish to report a state-of-the-art high speed OEIC receiver realized with a 0.6 μm gates direct ion implanted GaAs MESFET, and a 52 μm x 52μm MSM detector.

2. MATERIALS and DEVICE FABRICATION

The substrates used in this work were LEC-grown 3-inch semi-insulating GaAs (100) wafers. The conduction channel, resistor and source drain region was formed by direct Si^+ ion implantation. Wafers were subsequently annealed at 850 °C in a H_2/AsH_3 atmosphere without cap [5]. From a polaron profile measurement, the peak carrier concentration of 1.8×10^{18} cm^{-3} occurred at a depth of 0.08 μm. A carrier concentration of 1.3×10^{18} cm^{-3}, sheet resistance of 200 ohms per square, 300 K mobility of 1000 $cm^2/V \cdot s$ were obtained at room temperature from Hall measurements. Mesa isolation of the active areas for FETs and resistors were done by wet chemical etching. The source/drain and the 0.6 μm gate electrodes were formed by AuGe/Ni/Au and Ti/Pt/Au, respectively. The drain to source

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saturation current, I_{dss} = 150 mA/mm, and the pinch-off voltage, V_p = -1.2 V. The transconductance is 195 mS/mm at V_{gs} = 0 V and V_{ds} = 1.5 V with the peak value of 275 mS/mm at V_{gs} = 0.7 V and V_{ds} = 1.5 V.

The unity current gain cutoff frequency, f_T, extrapolated from $|H_{21}|$ using -6 dB/octave slope, is 28 GHz without correction and is 34 GHz with a pad capacitance correction for a 0.6 μm x 100 μm gate MESFET. The gate-source and gate-drain capacitance were determined by the small signal model from measured S-parameters to be C_{gs} = 84 fF and C_{gd} = 15 fF respectively. The area of the MSM photodetector is 52 μm x 52 μm, with a 2 μm line by 3 μm spacing. The MSM capacitance is estimated to be 32 fF. A scanning electron micrograph of the OEIC receiver is shown in Fig. 1.

3. NOVEL CIRCUIT DESIGN

The transimpedance amplifier is designed to achieve high bandwidth using negative feedback . Transimpedance amplifiers are in general less sensitive to the process related variations and therefore make it more suitable for monolithic integration. Our receiver consists of an MSM detector, a transimpedance stage, and an output buffer stage, as shown in Figure 2. The transimpedance stage provides high voltage gain, while the output buffer stage provides current gain. The -3 dB frequency response of the transimpedance amplifier can be expressed as,

$$f_{-3dB} = \frac{(1+A_0)}{2\pi \times R_f\left[\left(1+{A_0}/{g_m R_f}\right)(C_{gs}+C_d)+(1+A_0)C_{gd}\right]}$$

where A_o is the open loop gain, g_m is the transconductance of transistor Q_1 and C_d is the input capacitance of the photodetector. As can be seen from this equation, the bandwidth of the receiver can be improved by decreasing C_d and R_f. However, if the area of photodetector is made too small in reducing C_d, the dynamic range will degrade due to the low input photocurrent.

The feedback resistance is 1.0 KΩ. Since the resistance is also the source of Johnson noise, the resistance selection is determined from the trade-off between the equivalent input noise current and bandwidth of the transimpedance. For the high frequency receiver design, R_f should made small, but at the expense of gain reduction. The output driver is adjusted to provide 50 Ω output matching and can be easily interfaced to GaAs DCFL logic circuits. The impedance matching is achieved with a gate width of 100 μm for Q11 and Q12. The power supplies V_{d2} and V_s are 3.0 V and -2.0 V respectively. In order to improve the phase margin, we introduced an additional buffer stage. The added source follower stage, with small geometry transistors, reduces the parasitic loading at the feedback node. As a result, the phase delay around the feedback loop is minimized. This novel circuit design has achieved a phase margin of 75 degrees, whereas the conventional circuit configuration [1-3] achieved only a 55^o phase margin.

This improvement is crucial for high speed applications where stability is required at high frequency operation. DC I-V characteristics and scattering parameters of the GaAs MESFET (0.5 to 25 GHz) were used to extract the component values of a Curtice large signal MESFET model. Simulated OEIC receiver results with and without MSM capacitance are shown in Fig. 3. The -3 dB bandwidth of the transimpedance amplifier as determined by the simulation is 17.5 GHz. The -3 dB bandwidth of the OEIC receiver with 32 fF MSM capacitance was determined to be 12.5 GHz from the simulation. This simulated result is comparable with the experimental measurement of 11 GHz as shown in Fig. 5.

4. OEIC RECEIVER PERFORMANCE

The OEIC receiver was characterized using a Cascade Microtech high frequency on-wafer probe. The MSM photo diode was irradiated by a 35 ps optical pulse stream with a 1 MHz repetition rate at a wavelength of 850 nm from a Tektronix OIG-501 optical impulse generator. The receiver output is connected to the input of a 40 GHz bandwidth Tektronix SD-30 sampling head. The optical input pulse and the measurement system were calibrated using a 60 GHz bandwidth photo detector module (Model 1002, New Focus, Inc.). The time domain pulse response of the OEIC receivers were measured at $\lambda = 850$ nm and the result is shown in Fig. 4. The bias conditions for optimum receiver performance are $V_{d1} = 6$ V, $V_{d2} = 2$ V, and $V_s = -1$ V. The FWHM of the receiver output pulse is 57 ps. The origin of the ringing shown in Fig. 4 is considered to be related to the input impedance mismatch between the MSM and the MESFET. The ringing is only 13% of the peak signal. The consequence of the ringing results in a small dip in the low frequency response and a lower -3 dB cutoff frequency of the OEIC receiver. The measured -3 dB bandwidth is 13 GHz when this ringing is excluded from the frequency response. This result is in excellent agreement with the corresponding simulation shown in Fig. 3. The measured frequency response of the OEIC receivers is shown in Fig. 5. A -3 dB bandwidth of 11 GHz is measured, which is good for 14 Gb/s NRZ operations. The transimpedance gain is 55 dBΩ. To our knowledge, both the bandwidth of 11 GHz and the transimpedance-bandwidth (TZBW) product of 6.1 THz-ohm are the best reported results of GaAs MESFET or HEMT OEIC receivers.

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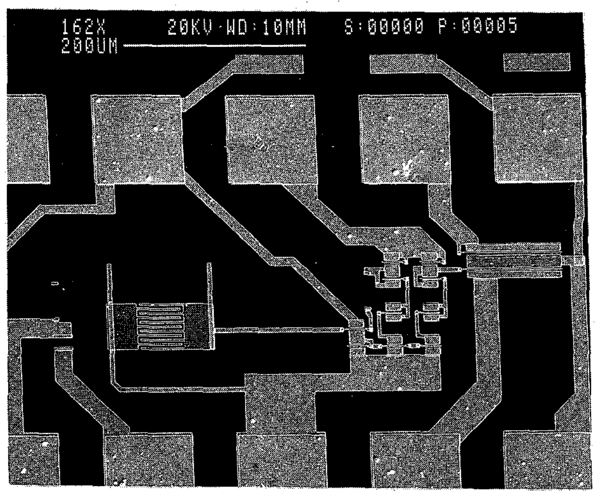

Figure 1. A SEM photograph of the fabricated GaAs MSM/MESFET OEIC receiver.

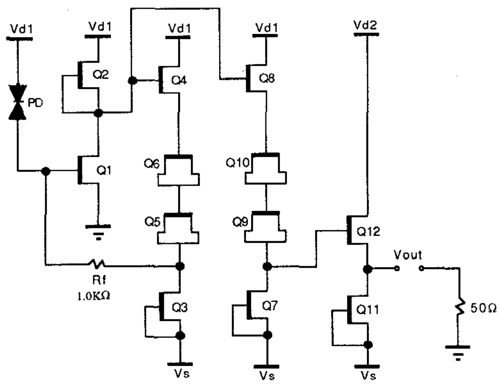

Figure 2. The OEIC circuit diagram.

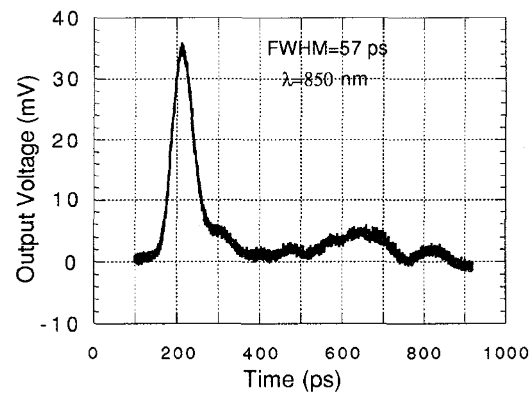

Figure 4. Output pulse response of the OEIC receiver to a 35 ps optical input pulse.

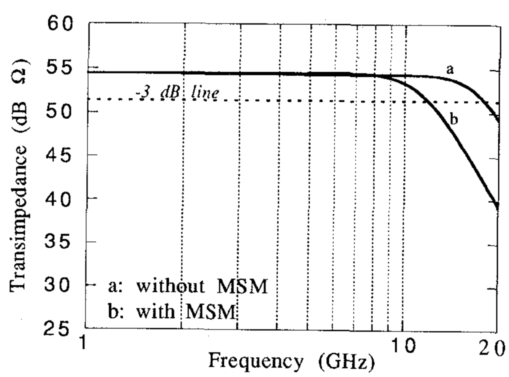

Figure 3. Simulation results of the bandwidth of OEIC receivers with and without the MSM photo detector, for a=0 fF and b=32fF.

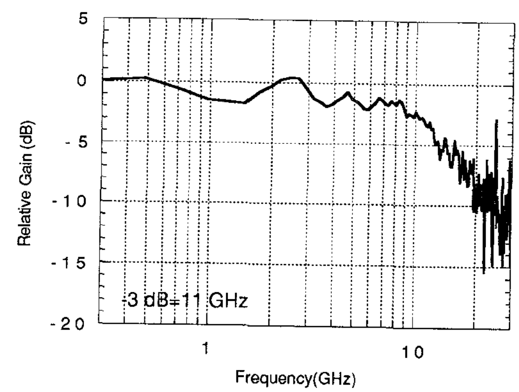

Figure 5. Relative frequency response of the OEIC receiver determined from Fourier transformations of output pulse response in Fig. 4.